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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT	:	Cornelius Van Zon			
SERIAL NO.	:	09/650,200	EXAMINER	:	Anand S. Rao
FILED	:	August 29, 2000	ART UNIT	:	2613
FOR	:	SYSTEM AND METHOD FOR DYNAMIC ADAPTIVE DECODING OF SCALABLE VIDEO TO BALANCE CPU LOAD			

APPEAL BRIEF TRANSMITTAL LETTER

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA. 22313-1450

Dear Sir:

Appellants respectfully submit three copies of an Appeal Brief For Appellants that includes an Appendix with the pending claims. The Appeal Brief is now due on May 11, 2005.

Appellants enclose a check in the amount of $500.00 covering the requisite Government Fee.

Should the Examiner deem that there are any issues which may be best resolved by telephone communication, kindly telephone Applicants undersigned representative at the number listed below.

Respectfully submitted,
Russell Gross
Registration No. 40,007

By: Steve Cha
Attorney for Applicant
Registration No. 44,069

Date: May 11, 2005

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Steve Cha, Reg. No. 44,069
(Name of Registered Rep.)

5/11/05
(Signature and Date)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	**Cornelius Van Zon**
Application No.	:	**09/650,200**
Filed	:	**August 29, 2000**
For	:	**SYSTEM AND METHOD FOR DYNAMIC ADAPTIVE DECODING OF SCALABLE VIDEO TO BALANCE CPU LOAD**

APPEAL BRIEF

On Appeal from Group Art Unit 2613

Date: May 11, 2005

Russell Gross
Registration No. 40,007
By: Steve Cha
Attorney for Applicant
Registration No. 44,069

Certificate of Mailing Under 37 CFR 1.8

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Steve Cha, Reg. No. 44,069
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5/11/05
(Signature and Date)

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TABLE OF CASES

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the present application, U.S. Philips Corporation, and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-21 have been presented for examination. All of these claims are pending, stand finally rejected, and form the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

In response to the patent application filed August 29, 2000, a first Office Action was mailed on April 4, 2004. Claims 1-21 were rejected under 35 USC §102(e) as being anticipated by Sethuraman (USP no. 6,434,196).

On July 7, 2004, a response to the first Office Action was timely filed which presented arguments why the reference cited failed to anticipate the claimed invention. Amendments were made to the claims to more clearly state the invention and to correct errors in form. On November 16, 2004, a second and Final Office Action was entered, which again rejected claims 1-21 as being anticipated by Sethuraman. On December 30,

2004 a response to the second and Final Office action was filed that presented additional arguments as to why the claimed invention was not anticipated by the recited reference.

An Advisory Action was mailed on March 1, 2005, which maintained the reason and provided further explanation for rejecting the claims. The Advisory Action stated that the amendments made to the claims were entered for the purposes of an appeal.

A Notice of Appeal, with appropriate fee, was filed on March 11, 2005. This Appeal Brief is being filed within two (2) months after the filing of the Notice of Appeal.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention describes a processing-load scalable video decoder contained in a receiving system comprising an analyzer circuit for monitoring at least one characteristic of an incoming video bit stream, generating at least one video parameter associated with the at least one characteristic and a processor load controller for receiving the at least one video parameter and controlling a level of decoding of the incoming video bit stream (p. 7, lines 7-15). More specifically, the scalable decoder receives a video bit stream, externally transmitted from an encoding transmitter and determines frame and source types using a bit stream analyzer that receives the incoming video bit stream and determines the level of motion and level of detail on a frame-by-frame basis (p. 18, lines 6-9). A process-work controller further receives video parameters from the scalable video decoder and bit stream analyzer and determines scale factors for controlling the processing work load according to a work load algorithm. In response to the scale factors, the video controller reduces the level of decoding during frames having a high level of motion or detail (p. 18, lines 9-21 and Figures 4 and 5).

VI. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

The issue in the present matter is whether:

1. Claims 1-21 are anticipated under 35 USC §102(e) by Sethuraman.

VII. ARGUMENT

I. Rejection of Claims 1-21 under 35 USC §102(e) as being anticipated by Sethuraman

Claims 1-21 stand rejected as being anticipated by Sethuraman as set forth in the Final Office Action mailed on 11/1/604. The Advisory Action provides further rationale for rejecting the claim by stating that "Sethuraman discloses that the encoding system [of Sethuraman] is capable of receiving an incoming scalable video bit stream ... Additionally, it is noted that since the embedded decoder is part of a pipelined architecture including an encoder, such an arrangement allows for concurrent processing using the 'embedded decoder' under the control of the pre-processing units... Furthermore, the 'embedded decoder' of the reference seems to read on the 'decoder' of the recited receiving apparatus, especially the 'decoding' occurs as a sub-function triggered by preceding processing, making the decoder as recited function as an 'embedded decoder' as in Sethuraman. The rate control as discussed in Sethuraman would have priority over both the encoding and decoding functions of Sethuraman, and thus, although primarily described in rate control for encoding, this function would also govern the decoding function of the pre-processing units, as well."

Difference Between the Claimed Invention

and the Primary Reference – Sethuraman

The instant invention, as recited in claim 1, which is typical of the remaining independent claims, recites:

> 1. An apparatus in a receiver that is configured for receiving and decoding an incoming scalable video bit stream that has been encoded by a transmitter for transmission externally from the transmitter and further configured for generating a baseband video signal, the apparatus being configured for controlling a processing load of said scalable video decoder, the apparatus comprising:
>
> an analyzer circuit configured for measuring, from the received bit stream, at least one characteristic of said received bit stream and generating at least one video parameter associated with said at least on characteristic; and
>
> a processor load controller configured for receiving said at least one video parameter and, in response, controlling a level of decoding of said received bit stream performed by said scalable video decoder. (emphasis added)

Sethuraman teaches a method and apparatus for encoding a video information stream to produce an encoded information stream according to a group of frames (GOP) information structure. In one aspect the encoding method includes an encoder, a controller, for adapting the information structure in response to an inter-frame information discontinuity, and a pre-processor for identifying and generating an indicium of the inter-frame information discontinuity. Sethuraman teaches that the information in the bit stream may vary because of the discontinuity information and uses the controller module to controls the bit rate of the output information stream by an appropriate utilization level of an output buffer. The appropriate utilization level of the transmitter

output buffer is designed to prevent problems in a receiving system caused by the varying bit rate. (see col. 9, lines 36-41, "[An] important task of the rate control module is to insure that the bit stream produced by the encoder does not overflow or underflow an input buffer in a decoder (e.g., within a receiver or target storage device, not shown) receiving a transmission comprising the output information stream."). Also included in the encoding structure described for encoding the video stream are components that are able to "decode" portions of the encoded bit stream to allow for motion compensation. (see col. 35, lines 45-49).

Hence, Sethuraman discloses an encoding system that is capable of adjusting the amount of data transmitted to a receiver/decoder such that input buffers in the receiver/decoder do not underflow or overflow. (see col. 9, lines36-53). The encoding system further includes an embedded decoder for motion-compensation processing. Hence, the decoding system need only process the received signal and is not required to determine any processing load adjustments.

Sethuraman Fails to Anticipate the Claimed Invention

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added).

Contrary to the position stated in the Final Office Action and the Advisory Action, Sethuraman fails to disclose each and every element recited in claim 1. More specifically, the present invention describes a processing-load scaleable decoder in a system receiving an encoded bit stream transmitted externally from a transmitter and the

decoding system then decodes the received bit stream and determines processing load adjustments based on the parameters of the received bit stream.

Sethuraman fails to teach an apparatus in a receiver for decoding an encoded video stream or a circuit, in the decoder, for measuring from the received bit stream at least one characteristic of the received bit stream and determining a level of decoding based on parameters of the decoded received signal, as is recited in the claims.

Sethuraman cannot be said to anticipate claim 1 because Sethuraman does not disclose each and every element claimed.

In this case, applicant believes that the examiner has read features into the Sethuraman reference based on the teachings of the present invention. Applicant would note that the Advisory Action states that "the 'embedded decoder' of the reference seems to read on the 'decoder' of the recited receiving apparatus, especially the [as] the 'decoding' occurs as a sub-function triggered by preceding processing, making the decoder as recited function as an '... embedded decoder ..." (emphasis added).(see p. 3, lines 14-16, Advisory Action). However, the embedded decoder of included in an encoding/transmitting system of Sethuraman is not capable of determining processing-load adjustments.

In view of the above, applicant submits that claim 1 is patently distinguishable and allowable over the teaching of Sethuraman.

With regard to independent claims 9 and 17, these claims recite a video receiver and a method, respectively, for receiving and processing an input bit stream in a manner similar to the apparatus described with regard to claim 1 and have been rejected for the same reason used to reject claim 1. Accordingly, for the remarks made with regard to

claim 1, which are reassert, as if in full herein, applicant submits that these claims are also not anticipated by Sethuraman.

With regard to the remaining dependent claims, these claims depend from the independent claims, which have been shown to include subject matter not disclosed by and allowable over Sethuraman. Applicant respectfully submits that the dependent claims are allowable at least for their dependence upon an allowable base claims, without even contemplating the merits of the dependent claims for reasons analogous to that held by In re Fine, 837 F.2d 1071, 5 USPQ 2d 1596 (Fed. Cir. 1988) wherein if an independent claim is non-obvious under 35 U.S.C. §103(a), then any claim depending therefrom is non-obvious. In this case, the remaining claims depend from allowable based claims, and, hence, these claims contain subject matter not disclosed by Sethuraman.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of Sethuraman and respectfully requests this honorable board reverse the rejection of the claims.

VIII. CONCLUSION

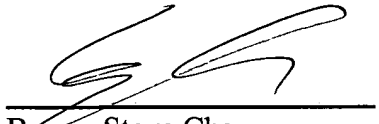
In view of the law and facts stated herein, it is respectfully submitted that the teachings of the primary reference, Sethuraman, fails to anticipate the claimed invention and the burden of showing that Sethuraman discloses all of the features, expressly or inherently, recited in the claims has not been met.

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render

obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Respectfully submitted,

Russell Gross
Registration No. 40,007



Date: May 11, 2005

By: Steve Cha
Attorney for Applicant
Registration No. 44,069

IX. CLAIMS APPENDIX

The claims on Appeal are as follows:

1. An apparatus in a receiver that is configured for receiving and decoding an incoming scalable video bit stream that has been encoded by a transmitter for transmission externally from the transmitter and further configured for generating a baseband video signal, said apparatus being configured for controlling a processing load of said scalable video decoder, said apparatus comprising:

an analyzer circuit configured for measuring, from the received bit stream, at least one characteristic of said received bit stream and generating at least one video parameter associated with said at least on characteristic; and

a processor load controller configured for receiving said at least one video parameter and, in response, controlling a level of decoding of said received bit stream performed by said scalable video decoder.

2. The apparatus as set forth in Claim 1 wherein said at least one video parameter indicates a level of motion of frames in said incoming scalable video bit stream.

3. The apparatus as set forth in Claim 1 wherein said at least one video parameter indicates a level of detail of frames in said incoming scalable video bit stream.

4. The apparatus as set forth in Claim 1 wherein said processor load controller is further configured for receiving a frame type parameter associated with a first frame in said incoming scalable video bit stream.

5. The apparatus as set forth in Claim 4 wherein said frame type parameter comprises at least one of an I-frame parameter, a B-frame parameter, and a P-frame parameter.

6. The apparatus as set forth in Claim 5 wherein said processor load controller is further configured for receiving a source type parameter associated with said first frame in said incoming scalable video bit stream.

7. The apparatus as set forth in Claim 6 wherein said source type parameter indicates whether said incoming scalable video bit stream is one of a video bit stream and a film bit stream.

8. The apparatus as set forth in Claim 1 wherein said processor load controller is configured to generate at least one scale factor for controlling a level of decoding performed by said scalable video decoder.

9. A video receiver comprising:

a buffer configured for receiving an incoming scalable video bit stream that has been transmitted externally from a video transmitter and for storing the received bit stream;

in communicative connection with the buffer, a scalable video decoder configured for decoding the bit stream that has been stored and generating a baseband video signal, said scalable video decoder comprising:

an apparatus configured for controlling a processing load of said scalable video decoder comprising:

an analyzer circuit configured for measuring at least one characteristic of said bit stream that has been stored and generating at least one video parameter associated with said at least one characteristic; and

a processor load controller configured for receiving said at least one video parameter and, in response, controlling a level of decoding performed by said scalable video decoder on said bit stream that has been stored; and

coupled to said scalable video decoder, a display configured for displaying said baseband video signal.

10. The video receiver as set forth in Claim 9 wherein said at least one video parameter indicates a level of motion of frames in said incoming scalable video bit stream.

11. The video receiver as set forth in Claim 9 wherein said at least one video parameter indicates a level of detail of frames in said incoming scalable video bit stream.

12. The video receiver as set forth in Claim 9 wherein said processor load controller is further configured for receiving a frame type parameter associated with a first frame in said incoming scalable video bit stream.

13. The video receiver as set forth in Claim 12 wherein said frame type parameter comprises at least one of an I-frame parameter, a B-frame parameter, and a P-frame parameter.

14. The video receiver as set forth in Claim 13 wherein said processor load controller is further configured for receiving a source type parameter associated with said first frame in said incoming scalable video bit stream.

15. The video receiver as set forth in Claim 14 wherein said source type parameter indicates whether said incoming scalable video bit stream is one of a video bit stream and a film bit stream.

16. The video receiver as set forth in Claim 9 wherein said processor load controller is configured to generate at least one scale factor for controlling a level of decoding performed by said scalable video decoder.

17. A method for controlling a processing load of a scalable video decoder incorporated within a receiver that receives an incoming scalable video bit stream from a transmitter configured for encoding to form said incoming scalable video bit stream and further configured for transmitting said incoming scalable video bit stream, said scalable video decoder being configured for decoding said incoming scalable video bit stream and generating a baseband video signal, said method comprising the steps of:

measuring, from the received bit stream, at least one characteristic of said received bit stream;

generating at least one video parameter associated with the at least one characteristic;

in response to a value of the at least one video parameter, controlling a level of decoding of the received bit stream performed by the scalable video decoder.

18. The method as set forth in Claim 17 wherein the at least one video parameter indicates a level of motion of frames in the incoming scalable video bit stream.

19. The method as set forth in Claim 17 wherein the at least one video parameter indicates a level of detail of frames in the incoming scalable video bit stream.

20. The method as set forth in Claim 17 further comprising the steps of:

determining a frame type parameter associated with a first frame in the incoming scalable video bit stream;

in response to a value of the at least one frame type parameter, controlling a level of decoding of the incoming scalable video bit stream performed by the scalable video decoder.

21. The method as set forth in Claim 20 wherein the frame type parameter comprises at least one of an I-frame parameter, a B-frame parameter, and a P-frame parameter.